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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,676	03/31/2000	Leslie E. Cline	42390.P7299	2061

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EXAMINER

LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
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2189

DATE MAILED: 03/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/540,676

Applicant(s)

CLINE, LESLIE E.

Examiner

Christopher E. Lee

Art Unit

2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION***Receipt Acknowledgement***

1. Receipt is acknowledged of the request filed 5th of March, 2003 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/540,676, which the request is acceptable and an RCE has been established. Claims 1, 8, 15 and 19 have been amended; no claims has been canceled; and no claim has been newly added. Currently, claims 1, 3-15 and 17-22 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3-11, 15 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. [US 6,131,134; hereinafter Huang] in view of Rafferty et al. [US 6,141,719 A; hereinafter Rafferty].

Referring to claim 1, Huang discloses a method, comprising: providing a first resistor (pull-up resistor 340 of Fig. 3) with a first end (i.e., the end coupled to switch 330 in Fig. 3) and a second end (i.e., the end coupled to D+ in Fig. 3), said first end coupled to a switch (switch 330 of Fig. 3) and said second end coupled to a data bus wire (USB interface D+ of Fig. 3) at a near of a data bus (See Fig. 3; i.e., detach control signal wire and switch 330, resistor 340 and data bus are located within USB converter 120 in Fig. 3); controlling (i.e., opening or closing) said switch with a detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3) to cause an apparatus (USB converter 120 of Fig. 3) containing said first resistor (i.e., resistor 340 of Fig. 3) and said switch (i.e., switch 330 of Fig. 3) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage is supplied to D+) makes said apparatus set said logically detached state); and switching (i.e., open or close said switch in Fig. 3) a

biasing voltage (i.e., 3.3V in Fig. 3) from said resistor (i.e., resistor 340 of Fig. 3) utilizing said switch (i.e., switch 330 of Fig. 3).

Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a data bus (i.e., bus 14 of Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58)

Referring to claim 8, Huang discloses an apparatus (USB converter 120 of Fig. 3), comprising: a first resistor with a first end and a second end (pull-up resistor 340 of Fig. 3); a switch (switch 330 of Fig. 3) coupled to said first end of said first resistor and a bias voltage (3.3V in Fig. 3); a detach control signal wire (switch controlling signal arrow from converting circuit 310 to switch 330 in Fig. 3) coupled to said switch at a near end of a data bus (See Fig. 3; i.e., detach control signal wire and switch 330, resistor 340 and data bus are located within USB converter 120 in Fig. 3), to receive a detach control signal (i.e., switch controlling signal from converting circuit 310 to switch 330 in Fig. 3) to cause said apparatus (i.e., USB converter) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage is supplied to D+) makes said apparatus set said logically detached state); and a data bus wire (USB

interface D+ of Fig. 3) of said data bus (USB interface D+ and D- in Fig. 3) coupled to said second end of said first resistor (See Fig. 3).

Huang does not teach said detach control signal wire of said data bus and said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a data bus (i.e., bus 14 of Fig. 3), which includes a detach control signal wire (i.e., HS select / LS select lines in Fig. 4 coupled to bus 14 of Fig. 3; See col. 3, lines 29-43; i.e., wherein in fact that the peripheral module translates data from the peripheral device to data for the bus, the desired downstream module translates the data from the bus to data for the desired downstream USB device, and the switches are operated via said HS select / LS select lines (i.e., detach control signal wire) in accordance with the peripheral module implies that said data bus includes said detach control signal wire (i.e., HS select / LS select lines)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Referring to claim 3, Huang discloses said first resistor is configured as a pull-up resistor (pull-up resistor 340 of Fig. 3).

Referring to claim 4, Huang discloses detecting said switching of said biasing voltage (See col. 6, lines 30-35).

Referring to claim 5, Huang discloses determining a logically detached state responsive to said detecting (See col. 6, lines 28-30).

Referring to claim 6, Huang discloses said detach control signal is responsive to a wake-up signal (transferred signals between a non-PnP interface and a USB interface; See col. 3, lines 17-20).

Referring to claim 7, Huang discloses said detach control signal (i.e., switch controlling signal) is asserted (i.e., state of switch controlling signal which causes switch 330 to be closed) when said wake-up signal (i.e., converted signal from the signals transferred between non-PnP interface and USB interface) is de-asserted (i.e., state of the converted signal which ultimately causes switch 330 to be closed).

Referring to claim 9, Huang discloses said switch may apply said bias voltage to said first end of said first resistor responsively to a detach control signal (switch controlling signal from converting circuit 310 in Fig. 3) on said detach control signal wire (See col.6, lines 23-27).

Referring to claim 10, Huang discloses said detach control signal is generated responsively to a wake-up signal (transferred signals between a non-PnP interface and a USB interface; See col. 3, lines 17-20).

Referring to claim 11, Huang discloses said data bus carries universal serial bus data (USB interface D+ of Fig. 3).

Referring to claim 15, Huang discloses an apparatus (USB converter 120 of Fig. 3), comprising: means for providing a first resistor with a first end and a second end (pull-up resistor 340 of Fig. 3) coupled to a switch (switch 330 of Fig. 3) and said second end coupled to a data bus wire (USB interface D+ of Fig. 3) at a near end of a data bus (See Fig. 3; i.e., switch 330, resistor 340 and data bus wire are located within USB converter 120 in Fig. 3); means for controlling said switch with a detach control signal (switch controlling signal from converting circuit 310 in Fig. 3) to cause said apparatus (USB converter 120 of Fig. 3) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage

is supplied to D+) makes said apparatus set said logically detached state); and means for switching a biasing voltage from said resistor utilizing said switch (See col. 6, lines 23-27).

Huang does not teach said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a data bus (i.e., bus 14 of Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a data bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Referring to claim 17, Huang discloses said apparatus of claim 15, further comprising means for detecting said switching of said biasing voltage (See col. 6, lines 30-35).

Referring to claim 18, Huang discloses said apparatus of claim 15, wherein said detach control signal is responsive to a wake-up signal (converted signal from the signals transferred between non-PnP interface and USB interface; See col. 3, lines 17-20).

Referring to claim 19, Huang discloses a system, comprising: a data bus (USB interface in Fig. 1 and 2) with a near end (side of USB converter 120 in Fig. 1) and a far end (side of computer system 110 in Fig. 1); a first circuit (USB converter 120 of Fig. 1), coupled to said near end (See Fig. 1), including a first resistor with a first end and a second end (pull-up resistor 340 of Fig. 3), a switch (switch 330 of Fig. 3) coupled to said first end of said first resistor and to a bias voltage (3.3V in Fig. 3), a data bus wire (USB interface D+ of Fig. 3) of said data bus (USB interface D+ and D- in Fig. 3) coupled to said second

end of said first resistor (See Fig. 3), a detach control signal wire (switch controlling signal arrow from converting circuit 310 to switch 330 in Fig. 3) coupled to said switch to receive a detach control signal (i.e., switch controlling signal) to cause said first circuit (i.e., USB converter) to enter a logically detached state (See col. 6, lines 27-30 and 50-67; i.e., in fact, even if said apparatus is physically connected (i.e., physically attached), the open switch (i.e., no voltage is supplied to D+) makes said first circuit set said logically detached state); and a second circuit (computer system 110 of Fig. 1), coupled to said far end (See Fig. 1).

Huang does not teach said detach control signal wire of said data bus and said logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device) sent from a far end of said data bus.

Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13-29) is sent from a far end (i.e., from a corresponding peripheral module; See col. 3, lines 26-28) of a data bus (i.e., bus 14 of Fig. 3), which includes a detach control signal wire (i.e., HS select / LS select lines in Fig. 4 coupled to bus 14 of Fig. 3; See col. 3, lines 29-43; i.e., wherein in fact that the peripheral module translates data from the peripheral device to data for the bus, the desired downstream module translates the data from the bus to data for the desired downstream USB device, and the switches are operated via said HS select / LS select lines (i.e., detach control signal wire) in accordance with the peripheral module implies that said data bus includes said detach control signal wire (i.e., HS select / LS select lines)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a data bus, as disclosed by Rafferty, in said first circuit, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e., logically attaching and detaching) of said apparatus (i.e., USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Referring to claim 20, Huang discloses said switch (switch 330 of Fig. 3) may apply said bias voltage (3.3V in Fig. 3) to said first end of said first resistor responsively to said detach control signal (switch controlling signal from converting circuit 310 in Fig. 3). Refer to col.6, lines 23-27.

Referring to claim 21, Huang discloses said detach control signal is sent in response to a wake-up signal (converted signal from the signals transferred between non-PnP interface and USB interface; See col. 3, lines 17-20).

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [US 6,131,134] in view of Rafferty [US 6,141,719 A] as applied to claims 1, 3-11, 15 and 17-21 above, and further in view of Decuir [US 5,781,028].

Referring to claim 12, Huang, as modified by Rafferty, discloses all the limitations of claim 12 except that does not teach said data bus carries IEEE-1394 bus data.

Decuir teaches a conventional bi-directional transmission line using an IEEE 1394 standard (Fig. 4), wherein said data bus (transmission line 51 of Fig. 4) carries IEEE-1394 bus data (See col. 2, lines 23-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said data bus wire, as disclosed by Decuir, to said data bus wire of said apparatus, as disclosed by Huang, for the advantage of a high speed of data transmission, which is well know to one of ordinary skill in the art at the time the invention was made.

5. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [US 6,131,134] in view of Rafferty [US 6,141,719 A] as applied to claim 1, 3-11, 15 and 17-21 above, and further in view of Takasu [JP 407058800 A].

Referring to claim 13, Huang, as modified by Rafferty, discloses all the limitations of claim 13 except that does not teach a second resistor with a first end and a second end.

Takasu teaches a second resistor (terminating register R_2 of Fig. 1) with a first end and a second end, said first end coupled to said data bus wire (transmission line 9 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said second resistor, as disclosed by Takasu, in said apparatus, as disclosed by Huang, so as to provide effective termination on said bus, which is well known to one of ordinary skill in the art at the time the invention was made.

Referring to claim 14, Takasu discloses said second end of said second resistor is coupled to signal ground (R_2 of Fig. 1 as a pull-down resistor; See col. 4, lines 30-31).

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang [US 6,131,134] in view of Rafferty [US 6,141,719 A] as applied to claims 1, 3-11, 15 and 17-21 above, and further in view of Pollard et al. [US 5,754,870 A; hereinafter Pollard].

Referring to claim 22, Huang, as modified by Rafferty, discloses all the limitations of the claim 22 except that does not teach said wake-up signal is sent by said first circuit.

Pollard teaches a wake-up signal (i.e., status output monitor signal 58 of Fig. 2) is sent by a first circuit (i.e., plug-in card 30 of Fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have sent a wake-up signal from a near end of a first circuit, as disclosed by Pollard, in said system, as disclosed by Huang, as modified by Rafferty, for the advantage of monitoring the operability of said near end of said bus (i.e., card-data link connector and remote data link 64 in Fig. 2; Pollard).

Response to Arguments

7. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant's argument with respect to "a detach control signal sent from a far end of said data bus to cause an apparatus containing said first resistor and said switch to enter a logically detached state". The Examiner brought Rafferty [US 6,141,719 A] reference in the rejection for

the limitations which are not provided by Huang and all of the other art cited (See the instant Office Action, Paragraphs 3 through 6, *Claim Rejections - 35 USC § 103*).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure
In regard to the USB device control, Hsu et al. [US 6,393,588 B1] disclose a test apparatus for testing function of a USB hub under the control of a USB host computer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

CEL/ *CEL*
March 19, 2003

[Signature]
MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100